CLAIMS

We claim:

1. A logic analysis system for a digital logic emulation system configured to model a digital system and operating in response to at least one emulation clock signal, the logic analysis system comprising:

a clock signal generator for generating a multiplexing clock signal; and

a multiplexing subsystem for transmitting logic values of logic signals from the digital logic emulation system to a logic analyzer, the multiplexing subsystem multiplexing multiple logic values on channels of the logic analyzer for cycles of the emulation clock in response to the multiplexing clock signal.

2. A system as described in Claim 1, wherein the multiplexing clock signal from the clock generator has a frequency that is higher than each one of the user clock signals.

3. A system as described in Claim 1, wherein the multiplexing subsystem transmits the multiplexing clock signal to the logic analyzer as a strobe signal.

4. A system as described in Claim 1, wherein the multiplexing subsystem is implemented in a reconfigurable logic system in which the digital logic emulation system is implemented.

5. A system as described in Claim 1, wherein the multiplexing subsystem transmits tag signals to the logic analyzer to identify the logic values being transmitted to the logic analyzer.

6. A system as described in Claim 1, wherein the multiplexing subsystem comprises:

a multiplexor circuit for receiving and then transmitting the logic values to the logic analyzer; and

a controller for controlling the multiplexor circuit to sample the logic signals to obtain the logic values and to transmit the logic values.

7. A logic emulation system including reconfigurable logic devices and an interconnect for transmitting logic signals between the logic devices, and being configured to comprise:

a digital logic emulation portion for modeling a digital system operating in response to at least one emulation clock signal; and

a logic analysis multiplexing portion for transmitting logic values of logic signals from the digital logic emulation portion to a logic analysis device.

8. A system as described in Claim 7, wherein the logic analysis multiplexing portion transmits multiple logic values on channels of the logic analysis device for cycles of the emulation clock signal.

9. A system as described in Claim 7, further comprising a clock signal generator for generating a multiplexing clock signal having a higher frequency than the emulation clock signal.

10. A system as described in Claim 9, wherein the logic analysis multiplexing portion multiplexes the logic values transmitted to the logic analysis device in response to the multiplexing clock signal.

11. A method for sampling digital signals from a digital logic emulation system configured to operate in a digital system having an emulation clock signal, the method comprising:

sampling selected digital signals within the emulation system;

collecting digital signal values associated with the sampled digital signals for cycles of the emulation clock signal; and

multiplexing multiple ones of the digital signal values to a logic analysis device for cycles of the emulation clock signal.

12. A method as described in Claim 11, further comprising:

generating a multiplexing clock signal; and

multiplexing of the digital signal values to the logic analysis device in response to the multiplexing clock signal.

13. A method as described in Claim 11, further comprising:

transmitting the multiplexing clock signal to the logic analysis device; and

triggering the logic analysis device in response to the multiplexing clock signal.

14. A method as described in Claim 11, further comprising demultiplexing the digital signal values received from the emulation system.

15. A method as described in Claim 14, further comprising displaying the demultiplexed signal values in association with the emulation clock signal.

16. A method as described in Claim 11, further comprising multiplexing of the digital signal values to the logic analysis device in response to a virtual clock signal of the emulation system.

17. A method as described in Claim 11, further comprising transmitting tag signals to the logic analysis device to identify the digital signal values being transmitted to the logic analysis device.

18. A method as claimed in Claim 17, further comprising demultiplexing the logic values in response to the tag signals and aligning the logic values to correspond to cycles of the emulation clock signal.

19. A method as claimed in Claim 17, further comprising triggering the logic analysis device at least in part in response to the tag signals.

20. A method for configuring a logic emulation system including reconfigurable logic devices and an interconnect for transmitting logic signals between the logic devices, the method comprising:

programming the logic emulation system to have a digital logic emulation portion for modeling a digital system operating in response to at least one emulation clock signal; and

programming the logic emulation system to have a logic analysis multiplexing portion for transmitting logic values of logic signals from the digital logic emulation portion to a logic analysis device.

21. A method as described in Claim 20, further comprising programming the logic emulation system to multiplex multiple logic values on channels of the logic analysis device for every cycle of the emulation clock signal.

22. A digital logic analysis system, comprising:

a target system for generating at least one target system clock signal and data signals;

a programmable emulation system for executing a logic design being responsive to the target system clock signal and the data signals and generating data signals to the target system, the emulation system including a clock signal generator for generating a multiplexing clock signal;

a logic analysis device connected to the emulation system for sampling logic signals within the emulation system;

a configuring device for programming the emulation system to execute the logic design and multiplex logic values of the logic signals to the logic analyzer for every cycle of the target system clock signal in response to the multiplexing clock signal.

23. A logic analysis system for a digital logic emulation system configured to model a digital system and operating in response to at least two emulation clock signals, the logic analysis system comprising:

a clock signal generator associated with each emulation clock signal for generating a multiplexing clock signal in response to the corresponding emulation clock signal; and

a multiplexing subsystem associated with each clock signal generator for transmitting logic values of logic signals from the digital logic emulation system to a logic analyzer, the multiplexing subsystem multiplexing multiple logic values on each channel of the logic analyzer for every cycle of the corresponding emulation clock in response to the corresponding multiplexing clock signal.